IN THE CLAIMS

Please amend the claims as follows:

Claims 1-7 (canceled)

8. (Previously Presented) A method for operating an integrated circuit (IC), the method comprising:

receiving a modulated radio frequency (RF) signal at an input terminal of the IC;

varying a local oscillator in the IC across a range of frequencies at a sweeping rate higher than a data rate of the modulated RF signal to generate a local oscillator output;

mixing the local oscillator output with the modulated radio frequency signal using a mixer in the IC to generate a frequency translated signal;

filtering the frequency translated signal using a filter in the IC to pass a selected range of frequencies as a modulated intermediate frequency (IF) signal; and

demodulating the modulated IF signal using a demodulator in the IC to generate a data output from the modulated RF signal.

9. (Previously Presented) The method of Claim 8, wherein the local oscillator comprises a divider, an RF oscillator, and a reference oscillator forming a phase-lock-loop (PLL), and wherein varying the local oscillator comprises:

generating a reference frequency using the reference oscillator;

dividing an output of the RF oscillator by a division factor provided by the divider to generate a divided frequency;

dynamically altering the division factor provided by the divider;

adjusting the output of the RF oscillator to cause frequency lock between the divided frequency and the reference frequency; and

providing the output of the RF oscillator as the local oscillator output.

10. (Previously Presented) The method of Claim 9, wherein generating the reference frequency comprises supplying a timing signal from a timing device to the reference oscillator, wherein the timing device is external to the IC.

11. (Previously Presented) The method of Claim 8, wherein the local oscillator comprises a divider and an RF oscillator, and wherein varying the local oscillator comprises dynamically altering a division factor provided by the divider, the division factor being applied to a frequency provided by the RF oscillator to sweep the local oscillator output through the range of frequencies.

12. (Previously Presented) A method for operating a radio receiver formed as a monolithic integrated circuit (IC), the method comprising:

supplying a control signal to a local oscillator in the monolithic IC to select an output from the local oscillator having either a fixed frequency or a varying frequency;

mixing an input radio frequency (RF) signal with the output from the local oscillator using a mixer in the monolithic IC to generate a frequency translated signal;

filtering the frequency translated signal using an intermediate frequency (IF) filter in the monolithic IC to generate an IF signal; and

demodulating the IF signal using a demodulator in the monolithic IC to generate a data signal.

13. (Previously Presented) The method of Claim 12, wherein the demodulator comprises a baseband filter, and wherein demodulating the IF signal comprises:

applying a first control signal to a first bandwidth selection pin of the monolithic IC to adjust a bandwidth of the baseband filter; and

filtering the IF signal using the baseband filter as a lowpass filter.

14. (Previously Presented) The method of Claim 13, wherein demodulating the IF signal further comprises applying a second control signal to a second bandwidth selection pin of the monolithic IC, wherein the first control signal and the second control signal determine the bandwidth of the baseband filter.

15. (currently amended) The method of Claim 12, wherein the ~~range of frequencies~~ the output from the local oscillator comprises a band of frequencies about 2-3% around a transmit frequency of the input RF signal.

16. (withdrawn) A method for operating a radio receiver formed as a monolithic integrated circuit (IC), the method comprising:

generating a reference frequency using a reference oscillator in the monolithic IC, the reference frequency being process and temperature independent; and

generating a bias signal from a bias signal generator in the monolithic IC using the reference frequency, the bias signal controlling the characteristics of various components within the radio receiver, and the bias signal having a value that is compensated for temperature and process variations.

17. (withdrawn) The method of Claim 16, further comprising:

generating a local oscillator signal using a local oscillator in the monolithic IC;

mixing an input radio frequency (RF) signal with the local oscillator signal using a mixer in the monolithic IC to generate a frequency translated signal;

amplifying the frequency translated signal using an intermediate frequency (IF) amplifier in the monolithic IC;

filtering the frequency translated signal using an IF filter in the monolithic IC to generate an IF filtered signal; and

biasing the local oscillator, the mixer, the IF amplifier, and the IF filter using the bias signal to achieve temperature and process independence for the local oscillator, the mixer, the IF amplifier, and the IF filter, respectively.

18. (withdrawn) The method of Claim 17, further comprising:

monitoring the IF filtered signal using an automatic gain control (AGC) circuit in the monolithic IC to generate a first AGC signal when a magnitude of the IF filtered signal is greater than a reference voltage; and

reducing a gain of the IF amplifier in response to the first AGC signal.

19. (withdrawn) The method of Claim 16, wherein generating the bias signal comprises:

adjusting a current provided by a current-controlled-oscillator (ICO) in a phase-locked-loop (PLL) in the bias signal generator until frequency lock is achieved between the PLL and the reference frequency; and

supplying the current provided by the ICO as the bias signal.

20. (Previously Presented) A method for operating a radio receiver formed as a monolithic integrated circuit (IC), the method comprising:

filtering an input radio frequency (RF) signal using an intermediate frequency (IF) filter circuit in an all-CMOS superheterodyne receiver in the monolithic IC to generate an IF filtered output; and

demodulating the IF filtered output using an all-CMOS demodulator in the monolithic IC to generate a digital data signal.

21. (Previously Presented) The method of Claim 20, further comprising performing logic functions on the digital data signal using a decoder in the monolithic IC to

generate binary data at a data output terminal of the monolithic IC.

22. (Previously Presented) The method of Claim 21, wherein performing logic functions on the digital data signal comprises performing a decoding operation involving a changing code scheme.

23. (Previously Presented) The method of Claim 20, wherein filtering the input RF signal comprises:

providing a timing signal from a timing device to a local oscillator (LO) circuit in the monolithic IC, the timing device being external to the monolithic IC;

generating a LO output signal based on the timing signal using the LO circuit;

mixing the input RF signal with the local oscillator (LO) output signal using a mixer in the monolithic IC to generate a frequency translated signal; and

filtering the frequency translated signal using an IF filter in the IF filter circuit.

24. (Previously Presented) The method of Claim 20, wherein the digital data signal has a DC component, the method further comprising filtering the DC component from the digital data signal using a low pass filter that includes a capacitor that is external to the monolithic IC.

25. (Previously Presented) The method of Claim 20, further comprising controlling a gain of the all-CMOS superheterodyne receiver using an automatic gain control (AGC) circuit that monitors a magnitude of the IF filtered output.

26. (Previously Presented) The method of Claim 20, further comprising providing a bias voltage to the all-CMOS superheterodyne receiver and the all-CMOS demodulator using a bias supply circuit.

27. (Previously Presented) The method of Claim 26, wherein the all-CMOS superheterodyne receiver and the all-CMOS demodulator are formed using a plurality of pFET transistors and a plurality of nFET transistors, each of the plurality of pFET transistors having a first threshold voltage and each of the plurality of nFET transistors having a second threshold voltage, and

wherein the bias voltage is approximately equal to the first threshold voltage plus the second threshold voltage.

28. (Previously Presented) The method of Claim 20, wherein the all-CMOS superheterodyne receiver comprises a local oscillator (LO), a mixer, and a sweep generator, and wherein filtering the input RF signal comprises:

generating a varying frequency output from a local oscillator in the all-CMOS superheterodyne receiver;

mixing the input RF signal with the LO output signal using a mixer in the all-CMOS superheterodyne receiver to generate a frequency translated signal; and

filtering the frequency translated signal using an IF filter in the IF filter circuit.

29. (Previously Presented) The method of Claim 28, wherein generating the varying frequency output from the local oscillator comprises varying a frequency of the local

oscillator at a rate higher than a data rate of the input RF signal.

30. (Previously Presented) The method of Claim 20, wherein the all-CMOS demodulator comprises an amplitude modulation (AM) demodulator or an ON-OFF keyed (OOK) demodulator.

31. (Previously Presented) The method of Claim 20, wherein the all-CMOS superheterodyne receiver is configured to operate in the ISM band.

32. (Previously Presented) The method of Claim 20, further comprising generating a bias signal for controlling filtering characteristics of the IF filter circuit, wherein generating the bias signal comprises:

generating a reference frequency using a reference oscillator in the monolithic IC;

generating a control signal to cause a phase locked loop (PLL) circuit in the monolithic IC to achieve frequency lock with the reference frequency; and

supplying the control signal to the IF filter circuit as the bias signal.

33. (Previously Presented) A method for decoding a radio frequency (RF) signal, the method comprising:

providing the RF signal to a monolithic integrated circuit (IC);

generating a local oscillator signal using an all-CMOS local oscillator in the monolithic IC;

mixing the local oscillator signal with the RF signal using an all-CMOS mixer in the monolithic IC to generate a frequency translated signal;

filtering the frequency translated signal using an all-CMOS filtering circuit in the monolithic IC to generate a filtered output; and

demodulating the filtered output using an all-CMOS demodulator in the monolithic IC to generate a digital data signal.

34. (Previously Presented) The method of Claim 33, wherein mixing the local oscillator signal with the RF signal comprises varying the local oscillator signal across a range of frequencies at a sweeping rate higher than a data rate of the RF signal.

35. (Previously Presented) The method of Claim 34, wherein varying the local oscillator signal comprises:

dividing an output of an RF oscillator in the local oscillator by a division factor to generate a divided frequency;

dynamically altering the division factor;

adjusting the output of the RF oscillator to cause the divided frequency to match a reference frequency; and

providing the output of the RF oscillator as the local oscillator signal.

36. (Previously Presented) The method of Claim 35, wherein the reference frequency is process and temperature independent, the method further comprising:

generating a control signal to cause a phase-locked-loop (PLL) circuit in the monolithic IC to achieve frequency lock with the reference frequency; and

providing the control signal as a bias signal to the all-CMOS local oscillator and the all-CMOS filtering circuit for controlling characteristics of the all-CMOS local oscillator and the all-CMOS filtering circuit.

37. (Previously Presented) The method of Claim 35, wherein adjusting the output of the all-CMOS RF oscillator comprises:

providing a phase-locked-loop (PLL) in the local oscillator that includes the RF oscillator; and

adjusting the output of the RF oscillator to achieve frequency lock between the divided frequency and the reference frequency.

38. (Previously Presented) The method of Claim 33, wherein mixing the local oscillator signal with the RF signal comprises maintaining the local oscillator signal at a fixed frequency.

39. (Previously Presented) The method of Claim 33, further comprising filtering a DC component from the digital data signal using a low pass filter that includes a capacitor that is external to the monolithic IC.

40. (Previously Presented) The method of Claim 33, further comprising controlling a gain of the all-CMOS filtering circuit using an automatic gain control (AGC) circuit that monitors a magnitude of the filtered output.

41. (Previously Presented) The method of Claim 33, wherein the all-CMOS local oscillator, the all-CMOS mixer, the all-CMOS filtering circuit, and the all-CMOS demodulator are formed using a plurality of pFET transistors and a plurality of nFET transistors, each of the plurality of pFET transistors having a first threshold voltage and each of the plurality of nFET transistors having a second threshold voltage, the method further comprises providing a bias voltage to the all-CMOS local oscillator, the all-CMOS mixer, the all-CMOS filtering circuit, and the all-CMOS demodulator using a bias supply circuit, the bias voltage being approximately equal to the first threshold voltage plus the second threshold voltage.

42. (Previously Presented) The method of Claim 33, wherein the all-CMOS filtering circuit comprises an intermediate frequency bandpass filter.

43. (Previously Presented) The method of Claim 33, wherein the all-CMOS filtering circuit comprises a lowpass filter.

44. (currently amended) The method of claim 33, further comprising providing the digital data signal to a decoder within the monolithic integrated circuit. ~~,~~

45. (Previously Presented) The method of claim 33, further comprising providing the digital data signal to a circuit integrated within the monolithic integrated circuit, said circuit being selected from the group of an arithmetic logic unit circuit, a processor circuit, and a programmable logic circuit.